IN THE CLAIMS

Claims 1, 3, 4, 7, 8, and 11-15 are amended herein. Claims 2, 6, 9, 10, and 16-39 are cancelled. Claims 40-59 are added. All pending claims and their present status are produced below.

1. (Currently Amended) A processing system ~~comprises~~ comprising:

a register file[[,]] having an input and an output;

a routing unit having a first input, a second input, and an output, the first input of the routing unit coupled to the output of the register file, the routing unit capable of assembling and selecting a data signal;

a Banyan switch having a first input, a second input, and an output, the first input of the Banyan switch coupled to the output of the routing unit, the Banyan switch capable of controlling information pathways and performing routing functions on the data signal; ~~and having a first input coupled to an output of the register file,~~ and

an arithmetic logic unit having an input and an output, the input of the arithmetic logic unit coupled to [[an]] the output of the Banyan switch and [[an]] the output of the arithmetic logic unit coupled to [[an]] the input of the register file.

2. (Canceled)

3. (Currently Amended) The processing system of claim [[2]] 1 wherein the arithmetic logic unit comprises:

a bitwise function unit ~~with an~~ having an input and an output, the input of the bitwise function unit coupled to the output of the Banyan switch[[,]];

a pipeline register having an input and an output, the input of the pipeline register coupled to [[an]] the output of the bitwise function unit[[,]]; and

an accumulator having an input and an output, the input of the accumulator coupled to [[an]] the output of the pipeline register and [[an]] the output of the accumulator coupled to the input of the register file.

4. (Currently Amended) The processing system of claim [[2]] 1 wherein the Banyan switch comprises N data inputs, and $\log_M(N)$ switching stages~~, N equal to $\log_M(w)$, w being an internal bitwidth of the switch, and each of the N switching stages having N/2 switching cells~~.

5. (Original) The processing system of claim 4 wherein M is selected from a group comprising 2 and 4.

6. (Canceled)

7. (Currently Amended) The processing system of claim 5 further ~~comprises~~ comprising a switch control unit having an input and an output, the output of the switch control unit coupled to [[a]] the second input of the Banyan switch.

8. (Currently Amended) The processing system of claim 7 further ~~comprises~~ comprising a constant generator having an input and an output, the output of the constant generator coupled to [[a]] the second input of the routing unit.

9. (Canceled)

10. (Canceled)

11. (Currently Amended) The processing system of claim [[9]] 1 wherein the routing unit comprises:

a control logic generating a control signal having groups of bits [[,]]; and

a plurality of logics respectively operating on the groups of bits.

12. (Currently Amended) The processing system of claim [[11]] 7 wherein the switch control unit comprises:

a shift constants generator[[,]] having an input and an output, the input of the shift constants generator coupled to the input of the switch control unit;

a pipeline flip-flop having an input and an output, the input of the pipeline flip-flop coupled to [[an]] the output of the shift constants generator[[,]]; and

a switch tree having an input and an output, the input of the switch tree coupled to [[an]] the output of the pipeline flip-flop, and the output of the switch tree coupled to the output of the switch control unit.

13. (Currently Amended) The processing system of claim [[2]] 1 further ~~comprises~~ comprising a constant generator having an output coupled to the ~~first~~ second input of the ~~switch~~ routing unit.

14. (Currently Amended) The processing system of claim 13 further ~~comprises~~ comprising a switch control unit having an input and an output, the output of the switch control unit coupled to the ~~first~~ second input of the Banyan switch.

15. (Currently Amended) The processing system of claim [[2]] 1 further ~~comprises~~ comprising a switch control unit having an input and an output, the output of the switch control unit coupled to [[a]] the second input of the Banyan switch.

16. – 39. (Canceled)

40. (New) The processing system of claim 4 wherein M is 2 and each of the switching stages has N/2 switching cells.

41. (New) A computer-implemented method of processing data for use with a system for routing and manipulating data, the method comprising:

receiving data;

selectively aligning and transferring the data;

selectively routing the data using a Banyan switch; and

performing arithmetic or logic functions on the data.

42. (New) The method of claim 41 wherein selectively routing the data includes performing bitfield manipulation operations on the data.

43. (New) The method of claim 41 wherein selectively routing the data includes shifting or rotating the data.

44. (New) The method of claim 41 wherein selectively routing the data comprises:

receiving N data inputs; and

routing the N data inputs in $\log_M(N)$ switching stages, where M is 2 or 4.

45. (New) The method of claim 44 wherein the stages have N/2 cells, the cells capable of transferring a data input from any input of the cell to any output of the cell.

46. (New) The method of claim 41 wherein selectively aligning and transferring the data comprises:

generating a routing control signal having groups of bits; and

operating on the groups of bits to control the aligning and transferring.

47. (New) The method of claim 41 wherein selectively aligning and transferring the data comprises transferring conjoined data, transferring a shifted positive constant, transferring a shifted two's-complemented constant, conjoining flag bits, transferring a sign-extended constant, or transferring a shifted signal.

48. (New) The method of claim 41 further comprising generating a switching control signal that specifies a routing operation or bitfield manipulation operation.

49. (New) The method of claim 48 wherein the routing operation or bitfield manipulation operation comprises a circular shift operation, a logical shift operation, or a data alignment.

50. (New) The method of claim 48 wherein generating a switching control signal comprises:

receiving an input code;

outputting a shift code derived from the input code; and

generating and outputting the switching control signal in response to the shift code.

51. (New) The method of claim 50 wherein the input code is a Rotate Left Circular (RLC) code.

52. (New) The method of claim 51 wherein the shift code is the RLC code, an inverted RLC code, a zoned RLC code, or a fixed RLC code.

53. (New) The method of claim 52 wherein the zoned RLC code includes a bit position shift indication.

54. (New) The method of claim 41 further comprising selectively generating and outputting constants or bitfield mask primitives.

55. (New) A processing system comprising:

means for receiving data;

means for selectively aligning and transferring the data;

a Banyan switch for selectively routing the data; and

means for performing arithmetic or logic functions on the data.

56. (New) The processing system of claim 55 wherein the Banyan switch comprises N stages for routing the data, the N stages each having N/2 means for transferring a signal from any input to any output.

57. (New) The processing system of claim 55 further comprising means for generating a switching control signal that specifies a routing operation or bitfield manipulation operation, the means for generating a switching control signal coupled to the Banyan switch.

58. (New) The processing system of claim 57 wherein the routing operation or bitfield manipulation operation comprises a circular shift operation, a logical shift operation, or a data alignment.

59. (New) The processing system of claim 57 wherein the means for generating a switching control signal comprises:

means for receiving an input code;

means for outputting a shift code derived from the input code; and

means for generating and outputting the switching control signal in response to the shift code.